

ATMEL

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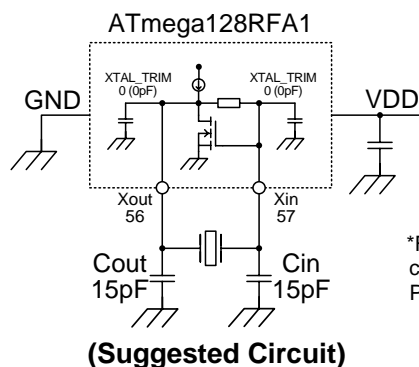
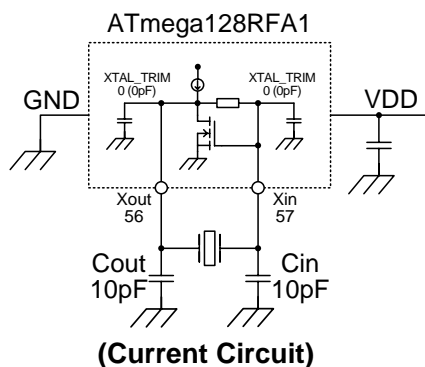
Thank you for your inquiry and we are pleased to report you our circuit analysis report as follows.

## Circuit Analysis Report

### 1. CONDITION

|              |                  |  |
|--------------|------------------|--|
| Test IC      | ATmega128RFA1    |  |
| Crystal      | Holder           | NX5032GA   |
|              | Frequency        | 16.000MHz  |
|              | Load capacitance | CL=8pF (Current)<br><b>CL=10pF (Suggested)</b>               |
|              | NDK Spec. No.    | STD-CSK-8(J) (*J:CL=10pF)                                    |
| Test Circuit | IC               | MEGA128RFA1-ZU 1105D 0T6227                                  |
|              | VDD              | +3V / +1.8V  |
|              | PCB              | TB3_MEGA_RF<br>AVR2067 - Crystal Characterization for AVR RF |

### 2. CIRCUIT DIAGRAM



\*For XTAL\_TRIM:0(0pF)  
connected PF0 to PB7 and  
PF1 was open (not connected)

### 3. RESULTS

- 1) This crystal unit requires negative resistance of  $-R = 700\Omega$  minimum for stable oscillation
- 2) Circuit characteristics

| Circuit   | Cout/Cin  | XTAL_TRIM<br>(Internal Cap) | Frequency deviation<br>dF/F                     | Negative<br>Resistance<br>-R | Drive Level<br>DL | Startup<br>time<br>Tstr |
|-----------|-----------|-----------------------------|---|------------------------------|-------------------|-------------------------|
| Current   | 10pF/10pF | 0 (0pF)                     | +8ppm (CL=8pF)                                  | 3060 $\Omega$                | Less than 10uW    | 1.5ms                   |
| Suggested | 15pF/15pF | 0 (0pF)                     | <b>+5ppm (CL=10pF)</b><br>Ref.: -34ppm (CL=8pF) | 1950 $\Omega$                | Less than 10uW    | 2ms                     |

- 3) Although the negative resistance of the current circuit is over our target, it seems too large.
- 4) In order to improve negative resistance, we recommend changing external capacitance values from Cout/Cin=10pF/10F to **Cout/Cin=15pF/15pF**. Besides, we recommend changing crystal load capacitance value from CL=8pF to **CL=10pF** in order to improve frequency deviation.